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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,008	07/09/2003	William K. Bischel	GEMF 2048-1	1018
22470	7590	02/24/2004	EXAMINER	
HAYNES BEFFEL & WOLFELD LLP P O BOX 366 HALF MOON BAY, CA 94019				KOCH, GEORGE R
		ART UNIT		PAPER NUMBER
		1734		

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/616,008	BISCHEL ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	George R. Koch III	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on \_\_\_\_.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-9 and 115-125 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-9 and 115-125 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 2, 4-9, 115-121, 124 and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US Patent 6,316,281 B1), Yamada et al (US Patent 5,621,837) and Haugsjaa et al (US 5,999,269).

As to claims 1 and 115, Lee discloses an optical assembly comprising an optical emitter chip (Figure 5, item 3), two integrated optics chip (items 4 and 6) and a submount (item 9). Lee discloses that the submount can have a standoff structure (items 20 and 21) protruding from the first surface of the submount. Lee discloses that one of the integrated optics chip (item 6) receives optical energy from the optical emitter chip (see column 5, lines 1-7 and column 5, line 59 to column 6, line 6). Lee also discloses bonding the optical emitter chip to a single standoff structure (see column 5, lines 39-51).

Lee does not disclose juxtaposing against the standoff structure or bonding to the submount the integrated optics chip that receives optical energy from the optical emitter chip. Lee is silent as to whether a pressing operation attaches the optical emitter chip against the standoff structure. Lee is also silent as to whether the emitter chip contacts the standoff structure in a first *plurality* of contact portions of the standoff structure, instead disclosing one contact portion for each standoff structure.

Yamada discloses juxtaposing against the submount an intergrated opto-electronics chip (item 67 in all Figures) which is associated with an optical emitter chip (item 37 or 62 in all figures, see column 21, lines 39-59, which indicates that the optical device can be an laser device or an LD array, i.e., Laser Device array). In one specific embodiment, (see Figure 43), standoffs (items 30) are used for juxtaposing the emitter

chip and opto-electronics chips. One in the art would appreciate that juxtaposing the integrated optics chip against the standoff structure or bonding the integrated optics chip to the submount allows for smaller packaging size, improving the value and ease of use of the optical assembly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have juxtaposed the integrated optics chip of Lee against a standoff structure as in Yamada and bonded the integrated optics chip as in Lee to the submount in order to improve the ease of use of the optical assembly.

Haugsjaa discloses juxtaposing against the standoff structure or bonding to the submount the integrated optics chip with both emitter and circuitry structures. Haugsjaa further discloses that the standoff structure can include multiple contact points (see, for example, Figure 2, which discloses 3 contact points for supporting an optical emitter array chip). Haugsjaa discloses that the standoffs allow for the height of the laser array device to be fixed a predetermined distance above the substrate (column 4, lines 1-9). Haugsjaa further discloses that proper alignment is critical for the proper functioning of the assembly (see column 1, line 14-27). Haugsjaa also discloses a pressing operation and apparatus (see Figure 3) that attaches the optical emitter chip against the standoff structure (see column 4, lines 36-43, which disclose movement of the array in all directions, which would comprises pressing into the substrate) using the same bonding technique as in Lee and Yamada (i.e., reflow soldering). One in the art would appreciate that the pressing and bonding steps as disclosed in Haugsjaa would allow for proper alignment of the two component structure of Haugsja, which is critical for proper functioning. Furthermore, one desiring to make a three component structure as

in Lee and Yamada would use the pressing and bonding steps of Haugsjaa for the application of each structure to the mount (or submount) in order to achieve proper alignment and proper functioning. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the pressing steps and alignment and multiple standoff structure as in Haugsjaa in the method of manufacturing an optical assembly as in Lee and Yamada as the pressing steps would improve functioning and the multiple contact point standoff structure improves height control of the emitter chip.

As to claims 2 and 116, Haugsjaa discloses that the standoff structures comprises a plurality of three segments as claimed (see Figure 2). Yamada also discloses using three segments in an embodiment (see Figures 43, 47 and 48), and Figure 43 of Yamada discloses that the standoff structure comprises a plurality of two segments which are mutually isolated from each other at least under said subject edge of said emitter chip, and which are arranged such that each segment includes a respective first portion which contacts the emitter chip (item 37) and a respective second portion which contacts the opto-electronics chip (item 67). One in the art would appreciate that contacting both the emitter and integrated optics chips on the portions of the standoffs provides for a stable platform and control of the height (i.e., z axis alignment) for both the emitter and integrated optics chip (such as item 67 of Yamada). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to allow for each standoff segment to have a portion that contacts the emitter

chip and a second portion in order to provide a stable platform and increased height control (i.e., z axis alignment).

As to claim 4, Haugsjaa discloses that the steps of pressing and bonding can be performed by flowing soldered and cooling the solder (see Figure 2, and column 4, lines 1-10). Solder only flows when heated and bonds only when cool.

As to claim 5, Haugsjaa as applied in claims 1, 2 and 4 disclose forming the solder bumps between said contact portions on said first submount (see Figure 2, submount is item 2, contact portions and standoffs are item 4, device is item 1, and the solder bumps are items 5).

As to claims 6, 7 and 117 the solder connections cited in Lee, Yamada, and Haugsjaa functions as an electrical conductive bonding material. Lee also discloses a number of electrical traces and contacts on the submount, some of which connect to the optical device and some which connect to the integrated chip. (see, for example, Lee, Figure 5, items 12, 22, and Figure 7q, items 86, 102, 63).

As to claim 8, 9, and 118 Lee discloses the possibility of using multiple lasers and detectors (i.e., emitters and integrated optics chips, see column 9, lines 27-36) but is silent as to the specific details. Haugsjaa as applied to claims 1, 2 and 4 discloses that all of the contact points for the single optical device (which is an emitter) being bonded are on the standoff structure. Furthermore, Haugsjaa as applied to claim 2 discloses at least three consecutive contact portions (for example, see Figure 2). Yamada and Haugsjaa disclose variants using an optical emitter array chip (see Figures 47 and 48 of Yamada, Figure 1 of Haugsjaa) as cited in claims 8 and 9. One in the art

would appreciate that using an optical emitter array chip technique as suggested by Yamada and Haugsjaa as the multiple laser suggested by Lee eliminates the need to space multiple single optical emitter chips on a submount and improve alignment accuracy for the entire system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized an array as in Yamada and Haugsjaa as such an element would reduce alignment errors and improve operating efficiency.

As to claim 119, Lee, Yamada and Haugsjaa, while disclosing juxtaposing (or aligning) prior to pressing and bonding, the references do not disclose deforming the integrated optic chip in the pressing stage. However, official notice is taken that it is well known and conventional to occasionally deform various components during bonding, especially when such components have warpage or other dimensional irregularities, or simply as a normal effect of the pressing operation disclosed. One would appreciate that in actual practice, while not ideal, when using an otherwise perfect but slightly deformed component, a moderate amount of deformation during the bonding would be required to ensure that the component is properly aligned for optical functioning, especially when used in conjunction with the alignment methods cited in Haugsjaa. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized conventional moderate deformation in order to properly bond and align the optical components.

As to claims 120-121, Lee discloses activating the optical emitter during the bonding of the monitor photodetector which monitors the emitter output (see for

example, column 5, lines 59-64). Furthermore, Lee, Yamada and Haugsjaa also provides support for using an array of optical emitter chips in the alignment (as discussed in claim 9 above).

As to claims 124 and 125 official notice is taken that the use of optical amplifiers in optoelectronic applications is well known and conventional. One in the art would appreciate that such an optical amplifier would improve optical functioning. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized an optical amplifier.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Yamada and Haugsjaa as applied to claim 1 above, and further in view of Feldman (US 6,235,141 B1)

Lee, Yamada and Haugsjaa do not disclose using an epoxy, but rather disclose using solder.

Feldman discloses using epoxy to bond structures in optoelectronics together. Feldman discloses that epoxy adhesives have a number of advantages over solder, including being less expensive, the capability of being bonded with or without heat, the epoxy material being resistant to oxidation, and the fact that selected epoxy adhesives can be transparent, which is especially useful for optical applications. One concerned with any of these factors due to the potential application of the optical assembly would be motivated to replace the solder of Lee, Yamada and Haugsjaa with an epoxy adhesive. Feldman also discloses the steps of applying, pressing (or attaching) and

curing the adhesive as claimed (see Figure 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized curable epoxy in the steps claimed over the solder of Lee, Yamada and Haugsjaa in order to achieve of the benefits of low cost, UV curing, oxidation resistant and transparency as needed.

6. Claim 122 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Yamada and Haugsjaa as applied to claim 115 above, and further in view of Sato (US 5,985,064) and Gaynes (US 6,129,804).

Haugsjaa as applied to claim 1 above discloses utilizing an apparatus to perform the step of pressing. From Figure 3, it appears that the apparatus has a chuck for holding the optic emitter array chip and a table for holding the submount. Haugsjaa is silent as to the further details of the apparatus. One in the art would appreciate that the details of any conventional chucking apparatus could be used.

Sato and Gaynes disclose similar apparatus for bonding electrical devices to mounts. Sato discloses a chucking system which holds a first chip against a surface of the chuck, then moves the chuck such that it contacts the appropriate location of the submount, and uses image recognition to achieve the appropriate alignment and presses the chuck down towards the submount or mounting surface until the chip contacts the appropriate location (see, for example, Figures 1 and 3) for improved accuracy in aligning the components. Furthermore, Gaynes discloses that it is known to make the chuck compliant in order to accommodate the thickness of the bonding

material and the substrate (see column 8, lines 49-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized a method in which a chucking apparatus performs the steps of affixing the first component (which would be the emitter array of Lee, Yamada and Haugsjaa) to a compliant surface of the chuck (as suggested by Gaynes), moving the chuck until the first component contacts the appropriate location of the second component (the standoff portion of the submount of Lee, Yamada and Haugsjaa) as such a method would improve the accuracy of alignment of the components and also be capable accommodating any random errors in the components or the bonding material.

7. Claim 123 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Yamada and Haugsjaa as applied to claim 115 above, and further in view of Blonder et al (US Patent 5,179,609).

The description of Lee is merely directed towards a single emitter chip and single optical fiber, but Lee does disclose that the techniques can be used to make systems with a plurality of waveguides, lasers, photodetectors and optical fibers (see column 9, lines 31-35) while being silent as the specific techniques for placing the multiple lasers and other structures on the mount. Haugsjaa discloses an embodiment using an optical emitter array chip and attaching an optical fiber array having a plurality of optical fibers (for example, see Haugsjaa, Figure 1 and column 3, lines 9-27). One in the art would appreciate that using an fiber optic array technique by placing spaced "v" grooves as suggested by Haugsjaa and hinted at by Lee improves alignment accuracy of the optical

fibers relative to the optical device such as a laser array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized a fiber optic array as in Haugsjaa as such an element would reduce alignment errors and improve operating efficiency. Furthermore, Lee, Yamada and Haugsjaa all attached a single fiber optic to the first submount, and Haugsjaa as applied further discloses attaching the optical fiber array to the first submount.

Lee, Yamada and Haugsjaa as applied to claim 115 does not disclose attaching each of said fibers in a longitudinally oriented v-groove in the undersurface of a fiber holder.

Blonder discloses attaching each of said fibers in a longitudinally oriented v-groove in the undersurface of a fiber holder (see, for example, Figure 6, item 60, called a lid). Blonder discloses that such a holder can be used to cover the fibers (column 2, lines 29-33). One in the art would appreciate that such a cover would protect the optical fibers at the point of connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilized a fiber holder such as that suggested by Blonder in order to improve the protection of the optical fiber at the point of connection to the optical assembly.

### ***Conclusion***

8. This is a continuation of applicant's earlier Application No. 09/784,687. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had

been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

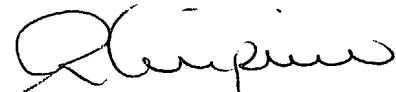
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George R. Koch III whose telephone number is (571) 272-1230 (TDD only). If the applicant cannot make a direct TDD-to-TDD call, the applicant can communicate by calling the Federal Relay Service at 1-800-877-8339 and giving the operator the above TDD number. The examiner can normally be reached on M-Th 10-7.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



George R. Koch III  
February 15, 2004



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